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Smirnova, Liudmila; Pyrhönen, Juha ; Iannuzzo, Francesco; Wu, Rui; Blaabjerg, Frede

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Round busbar concept for 30 nH, 1.7 kV, 10 kA IGBT non-destructive short-circuit tester

Liudmila Smirnova, Juha Pyrhönen
Lappeenranta University of Technology
Skinnarilankatu 34
Lappeenranta, Finland
E-Mail: Liudmila.Smirnova@lut.fi
URL: <http://www.lut.fi>

Francesco Iannuzzo, Rui Wu, Frede Blaabjerg
Aalborg University
Pontoppidanstrade 101
Aalborg, Denmark
E-Mail: fia@et.aau.dk
URL: <http://www.en.aau.dk/>

Keywords

«Bus bar», «Device characterization», «Modeling», «Power semiconductor device», «Reliability»

Abstract

Design of a Non-Destructive Test (NDT) set-up for short-circuit tests of 1.7 kV, 1 kA IGBT modules is discussed in this paper. The test set-up allows achieving short-circuit current up to 10 kA. The important objective during the design of the test set-up is to minimize the parasitic inductance and assure equal current sharing among the parallel connected devices. Achieving of a low inductance level is very challenging due to the current and voltage ratings, the presence of series and parallel protection systems and the required access for a thermal camera. The parasitic extractor Ansys Q3D is used to estimate the parasitic inductances during the design. A new concept of round-shaped, low inductive busbars for an NDT set-up is proposed. Simulation results verified that both reduction of overall inductance and good uniformity in current sharing among parallel devices are achieved by utilizing a circular symmetry. Experimental validation of the simulation was performed using a preliminary set-up. Further, this concept can be implemented in the design of the busbars for the power converters, where the parallel connection of the switching devices is applied to obtain higher current levels.

Introduction

The Non-Destructive Test (NDT) is a cost-effective solution used to test high power semiconductor devices at the edges of their Safe Operating Areas (SOA). The presence of the protection circuit allows preventing the failure of the Device Under Test (DUT) at the occurrence of any possible instable behavior. Thus, a lot of tests can be performed without damaging of an expensive high power device [1]. Moreover, this technique allows making results independent of parametric variations among the different devices.

During the design of an NDT for a very high current up to 10 kA, several aspects are needed to be taken into account. First, the stray inductance of the circuit provokes over/under voltages during transients and should, therefore, be minimized [2], [3]. The stray inductance also increases the turn-on time of the protection switches. Current and voltage ratings as well as the presence of series and parallel protections in the circuit are very challenging for achieving low inductance levels. Moreover, it is required by specification that during tests the temperature distribution inside the DUT is measured

with an infrared camera. This puts physical limitations on the design of the busbars since an access for the infrared camera is required in order to monitor the temperature during heavy loadings.

To minimize the inductance of the circuit, components with low stray inductances are used. Several components of the circuit are connected in parallel to obtain high current, so their equivalent inductance becomes low. To obtain a low inductive connection of the NDT circuit components, laminated busbars are used [4], [5]. In a busbar system, the copper plates are arranged in such a way that the currents in the nearby conductors flow in opposite directions forming as small flux producing surfaces as possible [6]. As the NDT is intended for a single-shot operation, the thickness of the conductive plates can be lower than in systems for continuous operation. However, the busbars are rather bulky due to the large dimensions of the high current and medium voltage components.

Another important issue which has to be considered during the design of the busbars is equal current sharing among parallel devices required for such high current levels. During fast transients, unequal current distribution may lead to the damage of the devices experiencing a higher current than the other devices connected in parallel. In this paper the design of 10 kA-rated busbars having 30 nH stray inductance and providing a current imbalance lower than 7 % among the parallel components of the circuit is presented. The inductance and the current distribution of the busbars are estimated using Ansys Q3D [7] and experimentally validated thanks to a preliminary setup.

Description of the NDT circuit

The aim of an NDT equipment is to perform short-circuit tests in the presence of a protection circuit able to turn-off the current very quickly right after the test. This capability allows saving the DUT by limiting the energy dissipated on it. It also allows performing repetitive tests. Even in the possible case of a rupture of the device, this technique avoids explosions, making them possible for post-failure analysis. Fig. 1 shows a classical NDT experiment.

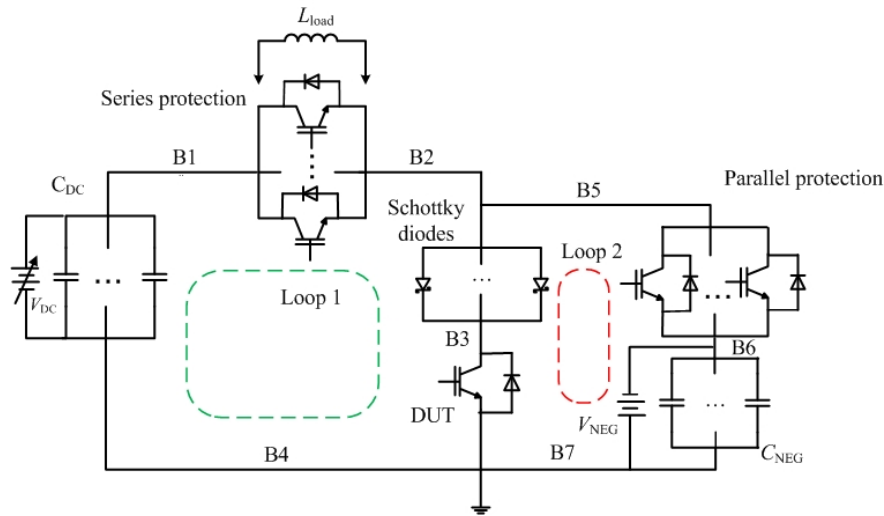


Fig. 1: Electrical schematic of the NDT set-up with the commutation loops 1 and 2. B1, B2, B3, B4, B5, B6, B7 indicates the busbars. DUT – Device Under Test.

The electrical schematic of the NDT with the commutation Loop 1 and Loop 2 is shown in Fig. 1. It includes the DUT, the series protection, parallel protection, load inductance L_{load} , DC link capacitance C_{DC} , a high voltage power supply V_{DC} , Schottky diodes, negative-voltage capacitance C_{NEG} with corresponding negative voltage supply V_{NEG} .

There are two different short-circuits types: type 1 happens during the IGBT turn-on, while type 2 happens when the IGBT is at on-state. The NDT can provide both short-circuit types by different configuration and control timing schemes. The timing control schemes of the NDT are illustrated as shown in Fig. 2, in which high state means on-state and low state means off-state.

For type 1 short-circuit, the load inductance in Fig. 1 should be removed. Before tests, series protection is on-state while parallel protection is off-state. During the tests, the DUT falls to short-circuit, when it is triggered. After the precise controlled time by 100 MHz FPGA, the DUT short-

circuit is switched off by series protection IGBTs. At the same time, the parallel protection is turned on to avoid any unwanted tail current through DUT. The corresponding control time sequences of series, parallel protections and DUT are as shown in Fig. 2 (a). The negative voltage V_{NEG} can speed up the parallel protection, and the Schottky diodes can avoid a current flow from the DUT to the negative voltage.

For type 2 short-circuit, the load inductance is required to obtain high current. At first, the series protection is off-state while DUT is turned on. In this case, the DUT conducts current determined by the load inductance. Then, the series protection is turned on and triggered an on-state short-circuit to DUT. Finally, short-circuit is ended with series protection turned off and parallel protection turned-on. The corresponding control time sequences of series, parallel protections and DUT are as shown in Fig. 2 (b).

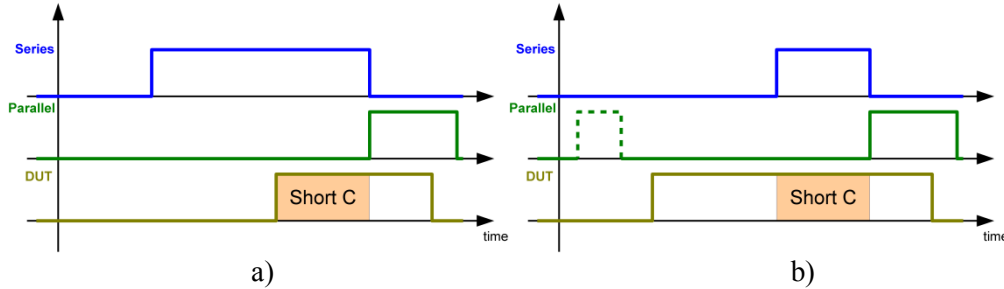
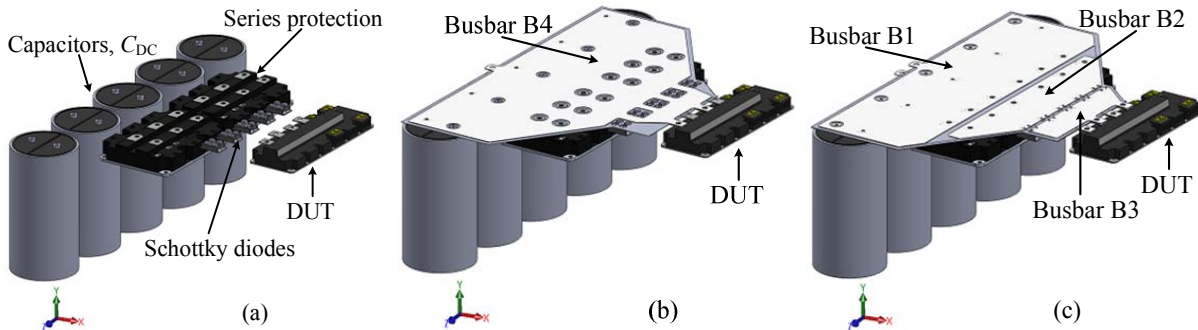


Fig. 2: Time sequences of the NDT signals. a) type 1 short circuit occurred during turn-on; b) type 2 short circuit occurred during conduction state.

Preliminary NDT set-up

At first, to tune up the simulation tool and validate the adopted approximations, the preliminary NDT set-up intended for short-circuit current up to 6 kA was built. It includes a series protection made up of two parallel 3300V 3000A IGBT modules, a parallel protection made up of two parallel 3300V, 2400A IGBT modules, the load inductance L_{load} , DC link capacitance C_{DC} consisting of five parallel capacitors, a high voltage power supply V_{DC} , five 170 V 1200 A parallel Schottky diodes, negative-voltage capacitance C_{NEG} consisting of three parallel capacitors with corresponding negative voltage supply V_{NEG} .

During the design of the NDT the inductances of the commutation Loop 1 and Loop 2 should be minimized in order to reduce the influence of short-circuit behaviour. First, focus is on Loop 1 which includes four copper busbars (B1 – B4) as presented in Fig. 1. In order to obtain a low inductance, the busbars in which the current flows in the opposite direction are placed close to each other, the distance is just the thickness of the insulation, which is 0.2 mm (Mylar). Two-layer busbars presented in Fig. 3 (b) - (c) are used. The bottom layer is the busbar B4 (Fig. 3 (b)) and the top layer includes the busbars B1, B2, and B3 (Fig. 3 (c)).



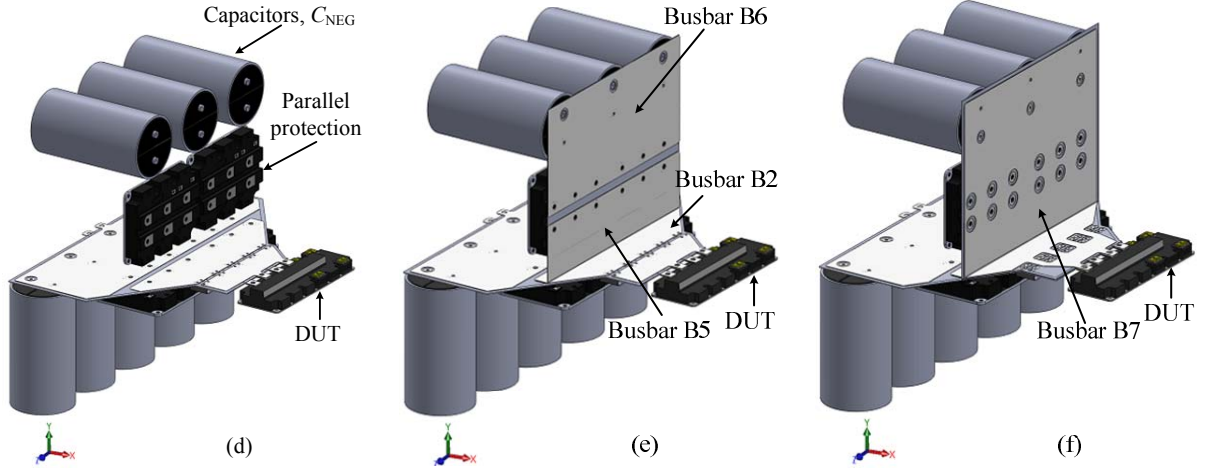


Fig. 3: 3D view of preliminary NDT set-up with the busbars of the Loop 1 and Loop 2.

Second, the design of the busbars of Loop 2 is considered. As shown in Fig. 3 (e) and (f) the busbars of the second loop are positioned in 90° angle with respect to the first one, which is done in order to allow measuring the temperature of an open DUT with a thermal camera looking at it from above. Loop 2 contains five copper busbars (B2, B3, B5, B6, and B7). In Fig. 4 the cross-section of the busbars is shown in false proportions; it can be seen that the thickness between the busbars of both commutation loops 1 and 2 is just the thickness of the insulation layer that leads to low parasitic inductance of both loops. A photograph of the assembled NDT set-up is presented in Fig. 5.

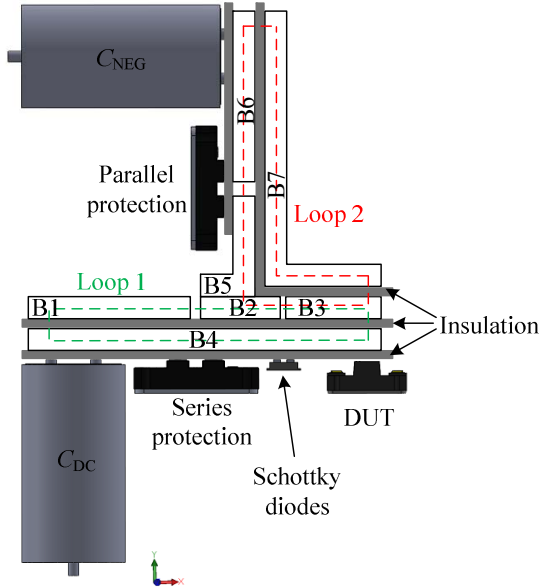


Fig. 4: Principal cross-section of the busbars with the commutation loop 1 and loop 2.

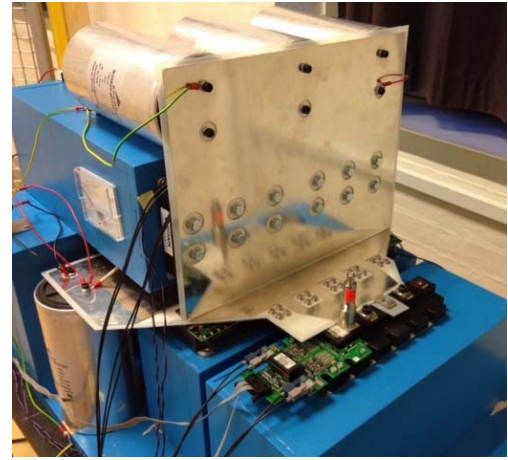


Fig. 5: Photograph of the preliminary NDT set-up.

The inductance of the busbars is estimated using Ansys Q3D. For AC inductance estimation a mesh with 10^6 triangle elements was created and is here omitted for brevity. According to the theory of partial inductance presented in [8] each component of the current loop can be characterized by self-partial and mutual partial inductances. The estimated self-partial and mutual partial inductances of the four busbars included in the commutation Loop 1 are presented in Table I.

Table I Self-partial and mutual partial inductances of the busbars B1, B2, B3, and B4 included in the commutation Loop 1 (at 1 MHz). The diagonal elements of the estimated partial inductance matrix ($L_{i,i}$) are the self-partial inductances of the busbars and the off-diagonal elements ($L_{i,j}$) are the mutual partial inductances.

Inductance [nH]	B1	B2	B3	B4
B1	6	0.7	0.3	-8.6
B2	0.7	4.3	0.65	-6.7
B3	0.3	0.65	5.4	-5.4
B4	-8.6	-6.7	-5.4	31

The net inductance of each busbar of the commutation loop, which presents the contribution of a component to an equivalent loop inductance, is calculated as [9]:

$$L_{\sigma i} = \sum_{j=1}^N \pm L_{\sigma i,j} \quad (1)$$

where N is a number of the busbars in the loop. The equivalent loop inductance of the busbars $L_{\sigma \text{busbars}1}$ is calculated as a sum of net inductances of the busbars included in Loop 1:

$$L_{\sigma \text{busbars}1} = \sum_{i=1}^N \sum_{j=1}^N \pm L_{\sigma i,j} \quad (2)$$

The calculated equivalent inductance of the busbars of Loop 1 is 8.6 nH. This value is lower than the sum of the self-partial inductances of the four busbars due to the presence of negative mutual inductances among the busbars. Similarly the inductance of the busbars of Loop 2 $L_{\sigma \text{busbars}2}$ is estimated to be 9.4 nH. The total inductances of the commutation Loop 1 ($L_{\sigma \text{loop}1}$) and Loop 2 ($L_{\sigma \text{loop}2}$) are obtained by

$$L_{\sigma \text{loop}1} = L_{\sigma \text{busbars}1} + L_{\sigma \text{DUT}} + L_{\sigma \text{Schottky}} + L_{\sigma \text{DCcaps}} + L_{\sigma \text{series_protection}} \quad (3)$$

$$L_{\sigma \text{loop}2} = L_{\sigma \text{busbars}2} + L_{\sigma \text{DUT}} + L_{\sigma \text{Schottky}} + L_{\sigma \text{NEGcaps}} + L_{\sigma \text{parallel_protection}} \quad (4)$$

where $L_{\sigma \text{DUT}}$ is the parasitic inductance of the DUT (10 nH), $L_{\sigma \text{Schottky}}$ is the equivalent parasitic inductance of five paralleled Schottky diodes (2 nH), $L_{\sigma \text{DCcaps}}$ is the equivalent inductance of five parallel DC capacitors (20 nH), $L_{\sigma \text{series_protection}}$ is the parasitic inductance of the series protection (5 nH), $L_{\sigma \text{NEGcap}}$ is the equivalent parasitic inductance of three capacitors forming the negative-voltage capacitance (33.3 nH), and $L_{\sigma \text{parallel_protection}}$ is the equivalent inductance of the parallel protection (5 nH). Fig. 6 shows the total loop inductances with the contribution of each component.

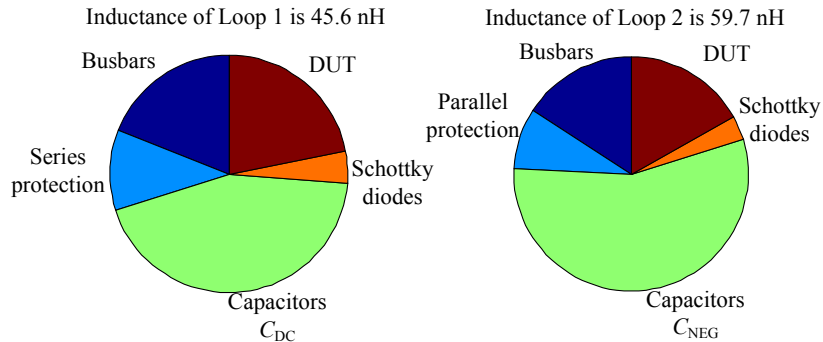


Fig. 6: Total parasitic inductances of Loop 1 and Loop 2 of the preliminary NDT set-up.

In order to verify the modeling results the voltage spike V_{spike} across DUT created by parasitic inductance (L_{loop1}) and current slope (di/dt) was measured (Fig. 7). The parasitic inductance of the commutation loop 1 can be then calculated

$$L_{\text{loop1}} = \frac{V_{\text{spike}} \cdot dt}{di} = \frac{(1248\text{V} - 900\text{V}) \cdot 36.8\text{ns}}{351.9\text{A}} = 37\text{ nH}. \quad (5)$$

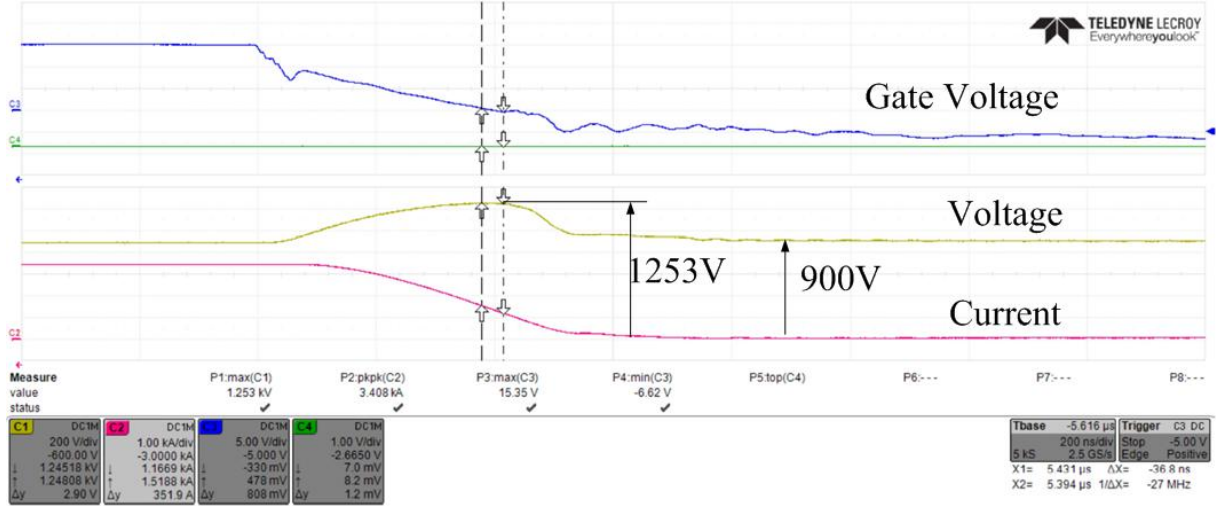


Fig. 7: Measured waveforms during turn-off of short-circuit current, CH1 - collector voltage, CH2 - collector current, CH3 - gate voltage.

In order to analyze the current distribution among the parallel devices in the layout shown in Fig. 5 the busbars of Loop 1 are modeled. The power devices in the model (Fig. 3 (c)) are replaced by copper stripes since the detailed models of the IGBT modules and Schottky diodes are not available. A model with $4.5 \cdot 10^5$ triangle mesh elements is used. Quite equal surface current distribution can be observed in Fig. 8.

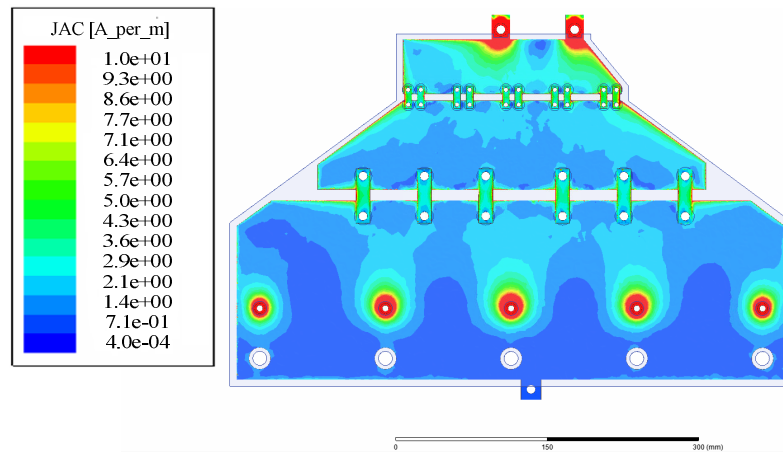


Fig. 8: Surface current distribution of the busbars of loop 1 at 1 MHz frequency with a total current of 1 A (the preliminary NDT set-up).

Final NDT set-up

The final NDT set-up is designed for short-circuit currents up to 10 kA. It includes the series protection made up of four parallel 3300V, 3000A IGBT modules, the parallel protection made up of four parallel 3300V, 2400A IGBT modules, the load inductance L_{load} , DC link capacitance consisting of ten parallel capacitors C_{DC} , a high voltage power supply V_{DC} , ten 170V, 1200A parallel Schottky

diodes, a negative-voltage capacitance consisting of eight parallel capacitors C_{NEG} with the corresponding negative voltage supply V_{NEG} .

Design of low inductive busbars – version 1

First, during the design of the busbars for the final NDT set-up, the same layout as for the preliminary NDT set-up (Fig. 3) is considered. Hence, two layer busbars presented in Fig. 9 are used for Loop 1, where the bottom layer is the busbar B4 and the top layer includes the busbars B1, B2, and B3.

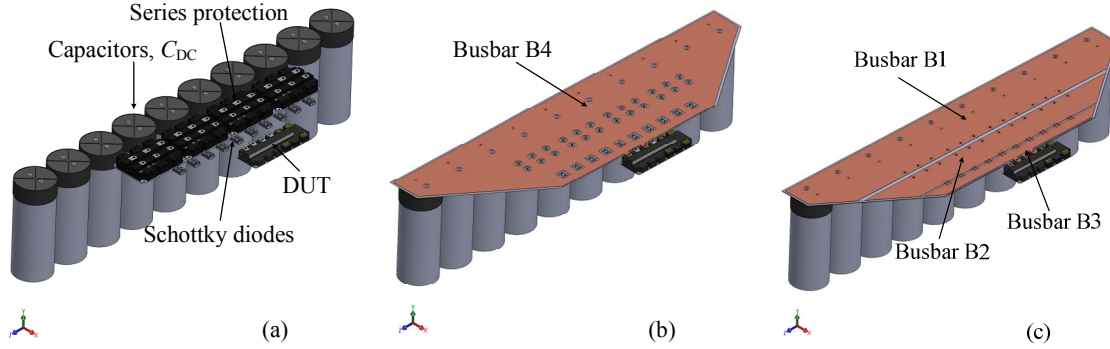


Fig. 9: A 3D view of version 1 of the final NDT with the busbars of the Loop 1.

The current distribution among the parallel devices in the layout shown in Fig. 9 is analyzed by modeling the busbars with the power devices being replaced by copper stripes. A model with $9 \cdot 10^5$ triangle mesh elements is used. Unequal surface current distribution can be observed in Fig. 10: the current is mostly concentrated in the middlemost devices (worst case current imbalance is 29 %) and may lead to their damage during a short-circuit test. Thus, the design of the final NDT set-up with the same layout of the busbars as for the preliminary set-up cannot be applied with reasonable results.

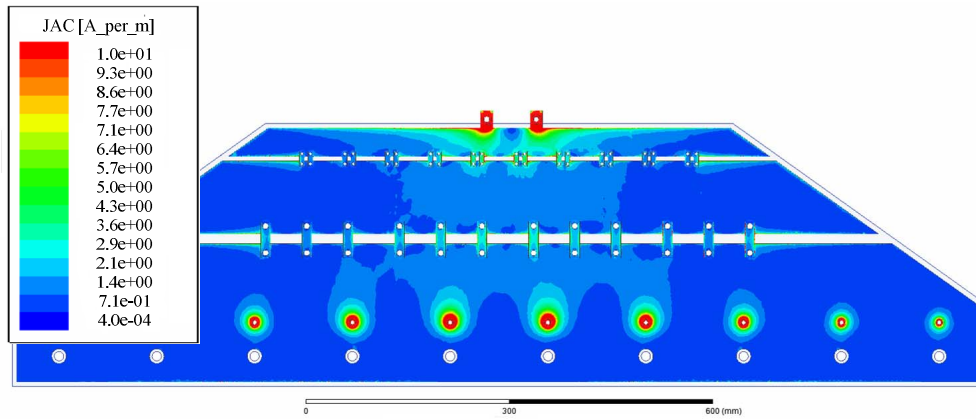


Fig. 10: Surface current density distribution of the busbars of Loop 1. The parallel components are short-circuited with copper stripes.

Design of low inductive busbars – version 2

In order to obtain a more uniform current distribution among the parallel devices, the circular layout presented in Fig. 11 is introduced. By focusing our attention again on Loop 1, the current distribution of the circular layout is presented in Fig. 12. It can be seen that the current distribution among the parallel devices is largely more uniform in the circular layout (current imbalance is 7 %) (Fig. 12) than in the traditional one (Fig. 10). Therefore, the circular layout demonstrates noticeable performance improvement from a current balancing point of view.

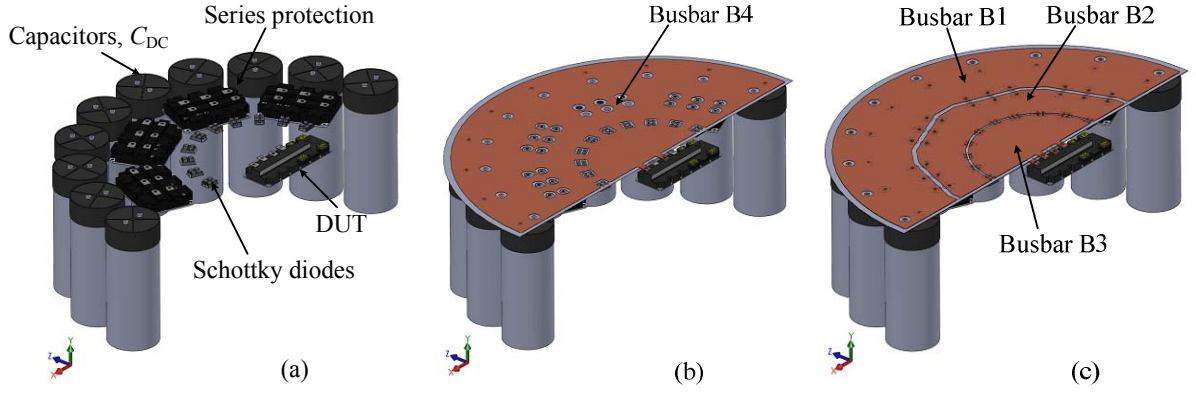


Fig. 11: 3D view of version 2 of NDT.

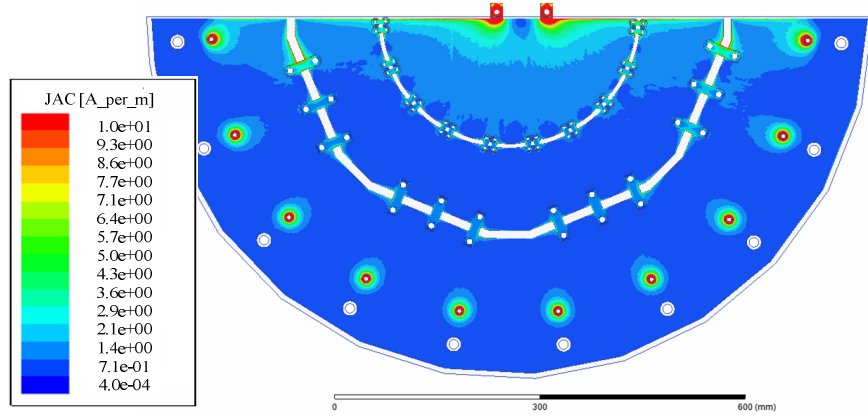


Fig. 12: Surface current density distribution of the busbars of the Loop 1. The parallel components are short-circuited with copper stripes.

The busbars of Loop 2 are 90° with respect to the busbars of Loop 1 as in the preliminary set-up (Fig. 13) to have an access for thermal camera. The cross-section of the busbars of the final set-up is similar to the preliminary set-up (Fig. 4).

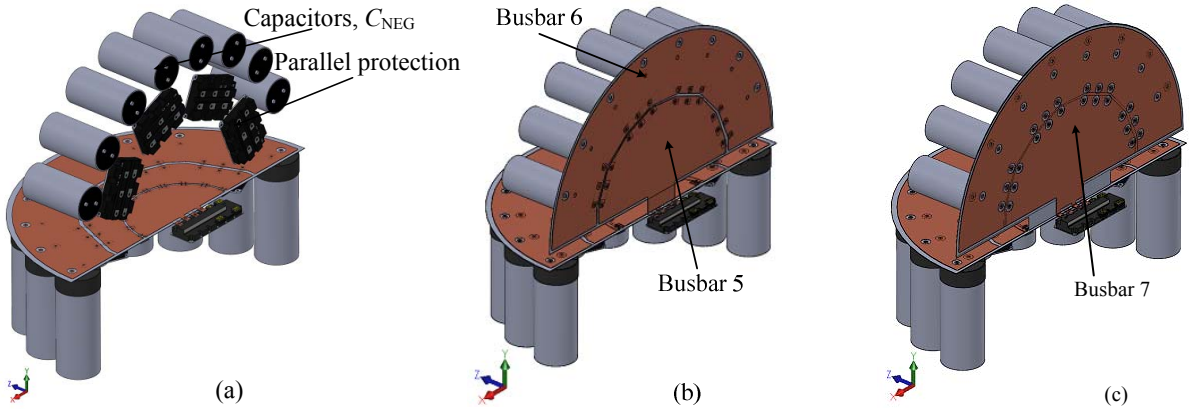


Fig. 13: 3D view of Non Destructive Tester (Loop 1 and Loop 2).

The inductances of the busbars are also estimated using Ansys Q3D. The inductances of Loop 1 and Loop 2 are calculated using (3) and (4). The inductance values of all components are presented in Table II where the inductance values of the power components are provided by the manufacturer and the inductances of the busbars are estimated. The total inductances of the loops are shown in Fig. 14, where the contribution of each component to the loop inductance is also presented.

Table II The stray inductances of the NDT components.

Component	Inductance [nH]
Capacitors C_{DC}	7
Capacitors C_{NEG}	12.5
Series protection	2.5
Parallel protection	2.5
Schottky diodes	1
DUT (module dependent)	10
Busbars of Loop 1	5.8 (Estimated using Q3D)
Busbars of Loop 2	6.6 (Estimated using Q3D)

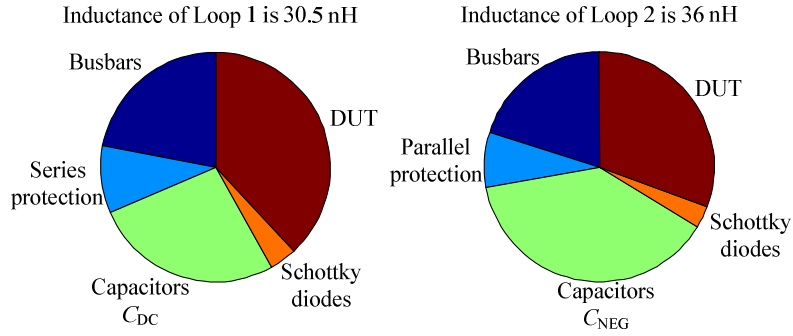


Fig. 14: Total inductances of the commutation Loop 1 and Loop 2.

Conclusions

In this paper a new design of the NDT set-up for short circuit tests of a high power IGBT module is proposed. The challenges associated with the design of the busbars for such a high current tests are discussed. The simulation results demonstrated that the circular symmetry of the layout introduced in this paper represents a breakthrough allowing an even current distribution in parallel devices. The low inductance of the busbars is achieved by laminating the busbars to enable currents flowing in opposite directions close to each other. The total inductances of the commutation loops are estimated to be around 30 nH, which is an unprecedented value for these kinds of high-voltage busbars. The busbars of Loop 2 required also 90° positioning in order to allow shooting by an infrared camera while keeping the inductances of the commutation Loop 1 and Loop 2 at such low values.

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